WHAT IS CLAIMED IS:

1. A digital/analog conversion device outputting an analog voltage according to digital data of a plurality of weighted bits, comprising:

a pulse number control circuit supplying, to a first node, pulses of a number according to said digital data, said pulses including a first transition edge changing from an initial level to a predetermined level and a second transition edge returning from said predetermined level to said initial level; and

a charge pump circuit changing, in a stepwise manner, each time one of said pulses is supplied to said first node, a voltage on an output node having an output capacitor connected thereto,

said charge pump circuit including

a pump capacitor connected between a second node and said first node,

a switch element connected between said second node and said output node to be turned on at a timing at which said first transition edge of each of said pulses is transmitted to said first node and turned off at a timing at which said second transition edge thereof is transmitted to said first node and

a bias circuit changing, according to the change of the voltage on said output node, a voltage on said second node with the same polarity as that of the change of the voltage on said output node.

2. The digital/analog conversion device according to claim 1, wherein

said pulse number control circuit includes

a switch circuit provided between a pulse node to which said pulses are successively supplied and said first node and transmitting, when said switch circuit is turned on, said pulses from said pulse node to said first node and

a switch control circuit turning on said switch circuit for a period of time according to said digital data.

3. The digital/analog conversion device according to claim 1, further comprising a precharge circuit for setting said first node, said second node and said output node each to a predetermined precharge voltage before said analog voltage is output.

4. The digital/analog conversion device according to claim 3, wherein

said precharge voltage corresponds to a minimum level in a range over which said analog voltage is controlled, and

said charge pump circuit increases in a stepwise manner the voltage on said output node each time said pulse is transmitted to said first node.

5. The digital/analog conversion device according to claim 3, wherein

said precharge voltage corresponds to a maximum level in a range over which said analog voltage is controlled, and

said charge pump circuit decreases in a stepwise manner the voltage on said output node each time said pulse is transmitted to said first node.

6. The digital/analog conversion device according to claim 1, wherein

said bias circuit includes a transistor electrically connected between a power-supply node to which a predetermined voltage is supplied and said second node, and

said transistor has its gate connected to said output node.

7. The digital/analog conversion device according to claim 1, wherein

said bias circuit includes

a first transistor of a first conductivity type electrically connected between a first power-supply node to which a first predetermined voltage is supplied and said second node,

a current-limiting element connected between a second power-supply node to which a second predetermined voltage is supplied and a third node and

a second transistor of a conductivity type opposite to said first conductivity type connected between a third power-supply node to which a third predetermined voltage is supplied and said third node,

said first transistor has its gate connected to said third node, and

said second transistor has its gate connected to said output node.

8. The digital/analog conversion device according to claim 7, wherein

said current-limiting element is constituted of a constant-current source supplying a constant current regardless of a voltage difference between said third power-supply node and said third node.

9. The digital/analog conversion device according to claim 1, wherein

said bias circuit includes

a first transistor of a first conductivity type and a second transistor of a second conductivity type opposite to said first conductivity type that are connected in series between a first power-supply node to which a first predetermined voltage is supplied and said second node,

a current-limiting element connected between a second power-supply node to which a second predetermined voltage is supplied and a third node and

a third transistor of said first conductivity type and a fourth transistor of said second conductivity type connected in series between a third power-supply node to which a third predetermined voltage is supplied and said third node,

said first transistor has its gate connected to said third node,

said fourth transistor has its gate connected to said output node, and

said second and third transistors are each diode-connected.

10. The digital/analog conversion device according to claim 9, wherein

said current-limiting element is constituted of a constant-current source supplying a constant current regardless of a voltage difference between said third power-supply node and said third node.

11. The digital/analog conversion device according to claim 1, wherein

said pump capacitor includes a plurality of first adjustment units connected in parallel between said first node and said second node,

said output capacitor includes a plurality of second adjustment units connected in parallel with respect to said output node,

said plurality of first adjustment units and said plurality of second adjustment units each include a unit capacitor and a link element connected in series, and

said link element is configured to be able to select, according to an input from the outside of said first and second adjustment units, whether or not to establish an electrical path including said unit capacitor correlated with said link element.

12. A display device displaying a gray level based on display data constituted of weighted n bits where n is an integer of at least two, comprising:

a plurality of pixel circuits each indicating a brightness according to a supplied voltage;

a selection line for selecting said plurality of pixel circuits;

a data line connected to said plurality of pixel circuits; and

a gray-level voltage generation circuit for supplying to said data line a gray-level voltage that is an analog voltage according to said display data,

said gray-level voltage generation circuit including

a pulse number control circuit supplying, to a first node, pulses of a number according to said display data, said pulses including a first transition edge changing from an initial level to a predetermined level and a second transition edge returning from said

predetermined level to said initial level and

a charge pump circuit changing, in a stepwise manner, each time one of said pulses is supplied to said first node, a voltage on an output node connected to said data line.

13. The display device according to claim 12, wherein

said charge pump circuit includes

a pump capacitor connected between a second node and said first node,

a switch element connected between said second node and said output node to be turned on at a timing at which said first transition edge of each of said pulses is transmitted to said first node and turned off at a timing at which said second transition edge thereof is transmitted to said first node and

a bias circuit changing, according to the change of the voltage on said output node, a voltage on said second node with the same polarity as that of the change of the voltage on said output node.

14. The display device according to claim 12, wherein

said charge pump circuit includes a pump capacitor for transmitting by capacitive coupling a voltage change on said first node caused upon said pulse is supplied, and

said pump capacitor is formed to have a similar configuration to that of a parasitic capacitance of said data line.

15. The display device according to claim 14, wherein

said pixel circuits each include a liquid-crystal element connected between a common electrode and a pixel node connected to said data line according to a state of said selection line,

a first insulating layer and a liquid-crystal layer having said liquid-crystal

element formed therein are deposited between a first metal interconnection layer having said data line provided therein and a layer having said common electrode formed therein,

a second insulating layer is present between a second metal interconnection layer having said selection line provided therein and said first metal interconnection layer,

said pump capacitor includes

a first electrode and a second electrode provided in said first metal interconnection layer,

a first dummy electrode formed in the layer in which said common electrode is formed in such a manner that said first dummy electrode is opposite to said first electrode with said liquid-crystal layer and said first insulating layer therebetween,

a second dummy electrode formed in said second metal interconnection layer in such a manner that said second dummy electrode is opposite to said first electrode with said second insulating layer therebetween,

a first contact portion formed in a through hole provided in said liquid-crystal layer and said first insulating layer for electrically connecting said first dummy electrode and said second electrode, and

a second contact portion formed in a through hole provided in said second insulating layer for electrically connecting said second dummy electrode and said second electrode, and

said pump capacitor has its capacitance represented by a synthetic capacitance value between said first electrode and said second electrode.

16. The display device according to claim 14, wherein

said pixel circuits each include a liquid-crystal element connected between a common electrode and a pixel node connected to said data line according to a state of said selection line,

a first insulating layer and a liquid-crystal layer having said liquid-crystal

element formed therein are deposited between a first metal interconnection layer having said data line provided therein and a layer having said common electrode formed therein,

a second insulating layer is present between a second metal interconnection layer having said selection line provided therein and said first metal interconnection layer,

said pump capacitor includes

a first electrode and a second electrode provided in said first metal interconnection layer,

a first dummy electrode formed in the layer in which said common electrode is formed in such a manner that said first dummy electrode is opposite to both of said first electrode and said second electrode with said liquid-crystal layer and said first insulating layer therebetween,

a second dummy electrode formed in said second metal interconnection layer in such a manner that said second dummy electrode is opposite to said first electrode with said second insulating layer therebetween,

an insulating film for allowing said second dummy electrode to stay in an electrically floating state, and

a contact portion formed in a through hole provided in said second insulating layer for electrically connecting said second dummy electrode and said second electrode, and

said pump capacitor has its capacitance represented by a synthetic capacitance between said first electrode and said second electrode.

17. The display device according to claim 12, wherein

said pixel circuits each include

a current-driven type light-emitting element indicating a brightness according to a supplied current and

a current-driving unit supplying to said current-driven type light-emitting

element a current according to said gray-level voltage supplied from said data line.

18. A display device displaying a gray level based on display data constituted of weighted n bits where n is an integer of at least two, comprising:

a plurality of pixel circuits each having a display element indicating a brightness according to a supplied voltage to said pixel circuit;

a data line connected to said plurality of pixel circuits; and

a gray-level voltage generation circuit for supplying to said data line a gray-level voltage that is an analog voltage according to said display data,

said gray-level voltage generation circuit including

a pulse control unit successively receiving pulses including a first transition edge changing from an initial level to a predetermined level and a second transition edge returning from said predetermined level to said initial level, and outputting said pulses or inverted pulses that are inverted versions of said pulses according to a specified bit among said n bits,

a pulse number control circuit receiving said pulses or said inverted pulses that are output from said pulse control unit, and transmitting, to a first node, said pulses or said inverted pulses of a number according to said display data,

a first charge pump circuit increasing, in a stepwise manner, in response to each of said pulses transmitted to said first node, a voltage on a first output node connected to said data line, and

a second charge pump circuit decreasing, in a stepwise manner, in response to each of said inverted pulses transmitted to said first node, a voltage on a second output node connected to said data line.

19. The display device according to claim 18, further comprising a precharge circuit precharging, before said gray-level voltage is generated, said data line to an intermediate voltage between a maximum level and a minimum level of said gray-level

voltage.

20. The display device according to claim 18, further comprising a precharge circuit precharging, before said gray-level voltage is generated, said data line to one of a maximum level and a minimum level of said gray-level voltage according to said specified bit.